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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,679	12/29/2000	Anthony X. Jarvis	00-BN-067 (STMI01-00067)	9128

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EXAMINER	
O'BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,679	JARVIS ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/29/00, 4/16/01 and 5/7/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-25 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration Fee as received on 4/16/2001 and Attorney Correspondence Address as received on 5/7/2001.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claim 11 is objected to because of the following informalities:

   a. Regarding claim 11, please arrange the claimed elements in a logical order. Specifically, the indented features of the "data processor" should be located under the element "data processor", rather than under the element "a plurality of memory-mapped peripheral circuits".

5. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3-4, 8-11, 13-14, 18-22 and 24-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Divivier et al., U.S. Patent No. 5,680,564.

8. Regarding claims 1, 11 and 21, taking claim 11 as exemplary, Divivier has taught a processing system comprising:

a. A data processor (see Fig. 1),

b. A memory coupled to said data processor (see Col.4 lines 47-49),

c. A plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor (see Col.15 lines 35-39, which incorporates by reference Shay, U.S. Patent No. 5,900,886, see Fig. 1), wherein said data processor comprises:

   i. An instruction execution pipeline comprising N processing stages (see Col.3 lines 22-23),

   ii. An instruction issue unit capable of fetching into said instruction execution pipeline instructions fetched from an instruction cache (16 of Fig. 1) associated with said data processor (see Col.4 lines 47-49), each of said fetched instructions comprising from one to S syllables (see Col.5 lines 1-4), said instruction issue unit comprising:

1. A first buffer (12 of Fig.1) comprising S storage locations capable of receiving and storing said one to S syllables associated with said fetched instructions, each of said S storage locations capable of storing one of said one to S syllables of each fetch instruction (see Col.3 lines 35-38),

2. A second buffer (14 of Fig.1) comprising S Storage locations capable of receiving and storing said one to S syllables associated with said fetched instructions, each of said S storage locations capable of storing one of said one to S syllables of each fetched instruction (see Col.3 lines 35-38),

3. A controller (20 of Fig.1, Col.3 lines 38-40) capable of determining if a first one of said S storage locations in said first buffer is full, wherein said controller, in response to a determination that said first one of said S storage locations is full, causes a corresponding syllable in an incoming fetched instruction to be stored in a corresponding one of said S storage locations in said second buffer (see Col.5 lines 40-51).

9. Claims 1 and 21 are nearly identical to claim 11. Claim 1 differs in its lack of a memory coupled to the data processor, and its lack of a plurality of memory-mapped peripheral circuits coupled to the data processor for performing selected functions in association with said data processor, but encompasses the same scope as claim 11. Claim 21 differs in it being a method

claim, but encompasses the same scope as claim 11. Therefore, claims 1 and 21 are rejected for the same reasons as claim 11.

10. Regarding claims 3 and 13, taking claim 13 as exemplary, Divivier has taught the processing system as set forth in claim 11, wherein S=8 (see Col.3 lines 35-36).

11. Claim 3 is nearly identical to claim 13. It differs in its parent claim, but encompasses the same scope as claim 13. Therefore, claim 3 is rejected for the same reasons as claim 13.

12. Regarding claims 4, 14 and 22, taking claim 14 as exemplary, Divivier has taught the processing system as set forth in claim 11, wherein S is a multiple of four (see Col.3 lines 35-36).

13. Claims 4 and 22 are nearly identical to claim 14. They differ in their parent claims, but encompass the same scopes. Therefore, claims 4 and 22 are rejected for the same reasons as claim 14.

14. Regarding claims 8, 18 and 24, taking claim 18 as exemplary, Divivier has taught the processing system as set forth in claim 11, wherein said controller is capable of determining when all of the syllables in one of said fetched instructions are present in said first buffer, wherein said controller, in response to a determination that said all of said syllables are present, causes said all of said syllables to be transferred from said first buffer to said instruction execution pipeline (see Col.3 lines 28-32 and Col.5 lines 1-16, 35-52).

15. Claims 8 and 24 are nearly identical to claim 18. They differ in their parent claims, but encompass the same scope as claim 18. Therefore, claims 8 and 24 are rejected for the same reasons as claim 18.

16. Regarding claims 9, 19 and 25, taking claim 19 as exemplary, Divivier has taught the processing system as set forth in claim 18, wherein said controller is capable of determining if a syllable in said first one of said S storage locations in said first buffer has been transferred from said first buffer to said instruction pipeline, wherein said controller, in response to a determination that said first one of said S storage locations has been transferred, causes said corresponding syllable stored in said corresponding one of said S storage locations in said second buffer to be transferred to said first one of said S storage locations in said first buffer (see Col.5 lines 35-52).

17. Claims 9 and 25 are nearly identical to claim 19. They differ in their parent claims, but encompass the same scope as claim 19. Therefore, claims 9 and 25 are rejected for the same reasons as claim 19.

18. Regarding claims 10 and 20, taking claim 20 as exemplary, Divivier has taught the processing system as set forth in claim 19, further comprising a switching circuit controlled by said controller and operable to transfer syllables from said second buffer to said first buffer (see Figs. 2 and 4, and Col.5 lines 35-52).

19. Claim 10 is nearly identical to claim 20. It differs in its parent claim, but encompasses the same scope as claim 20. Therefore, claim 10 is rejected for the same reasons as claim 20.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 2, 5-7, 12, 15-17 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Divivier et al., U.S. Patent No. 5,680,564.

22. Regarding claims 2 and 12, taking claim 12 as exemplary, Divivier has taught the processing system as set forth in claim 11, shown above, wherein S=8, but has not explicitly taught wherein S=4.

23. However, one of ordinary skill in the art would have recognized that decreasing the amount of usable syllables from 8 to 4 would not change the function of the processor, but would just decrease the number of usable syllables resulting in a scaling down of the hardware needed. Therefore, one of ordinary skill in the art would have found it obvious to modify Divivier to use 4 syllables instead of 8 syllables (see *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976)).

24. Claim 2 is nearly identical to claim 12. It differs in its parent claim, but encompasses the same scope as claim 12. Therefore, claim 2 is rejected for the same reasons as claim 12.

25. Regarding claims 5 and 15, taking claim 15 as exemplary, Divivier has taught the processing system as set forth in claim 11, shown above, wherein each of said one to S syllables comprises 8 bits (1 byte), but has not explicitly taught where each one of said one to S syllables comprises 32 bits.

26. However, one of ordinary skill in the art would have recognized that changing the bit size of a syllable from 8 to 32 bits would not change the function of the processor, but just increase the bit width (size) of the hardware that Divivier has already taught. Therefore, one of ordinary skill in the art would have found it obvious to modify Divivier to use 32 bit syllables instead of 8

bit syllables (see *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976), *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984,) and *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

27. Claim 5 is nearly identical to claim 15. It differs in its parent claim, but encompasses the same scope as claim 15. Therefore, claim 5 is rejected for the same reasons as claim 15.

28. Regarding claims 6 and 16, taking claim 16 as exemplary, Divivier has taught the processing system as set forth in claim 11, shown above, wherein each of said one to S syllables comprises 8 bits (1 byte), but has not explicitly taught where each one of said one to S syllables comprises 16 bits.

29. However, one of ordinary skill in the art would have recognized that changing the bit size of a syllable from 8 to 16 bits would not change the function of the processor, but just increase the bit width (size) of the hardware that Divivier has already taught. Therefore, one of ordinary skill in the art would have found it obvious to modify Divivier to use 32 bit syllables instead of 8 bit syllables (see *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976), *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), and *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

30. Claim 6 is nearly identical to claim 16. It differs in its parent claim, but encompasses the same scope as claim 16. Therefore, claim 6 is rejected for the same reasons as claim 16.

31. Regarding claims 7 and 17, taking claim 17 as exemplary, Divivier has taught the processing system as set forth in claim 11, shown above, wherein each of said one to S syllables comprises 8 bits, but has not explicitly taught where each one of said one to S syllables comprises 64 bits.

32. However, one of ordinary skill in the art would have recognized that changing the bit size of a syllable from 8 to 64 bits would not change the function of the processor, but just increase the bit width (size) of the hardware that Divivier has already taught. Therefore, one of ordinary skill in the art would have found it obvious to modify Divivier to use 32 bit syllables instead of 8 bit syllables (see *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976), *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), and *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

33. Claim 7 is nearly identical to claim 17. It differs in its parent claim, but encompasses the same scope as claim 17. Therefore, claim 7 is rejected for the same reasons as claim 17.

34. Regarding claim 23, Divivier has taught the method as set forth in claim 21, shown above, wherein each of said one to S syllables comprises 8 bits, but has not explicitly taught wherein each of the one to S syllables comprises one of: a) 16 bits, b) 32 bits, and c) 64 bits.

35. However, one of ordinary skill in the art would have recognized that changing the bit size of a syllable from 8 to 16, 32, or 64 bits would not change the function of the processor, but just increase the bit width (size) of the hardware that Divivier has already taught. Therefore, one of ordinary skill in the art would have found it obvious to modify Divivier to use 16, 32 or 64 bit syllables instead of 8 bit syllables (see *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976), *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), and *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

37. Riffe et al., U.S. Patent No. 4,502,111, has taught a method of aligning variable length instructions by breaking the instructions into byte-long tokens and transferring the tokens between sequential registers.

38. Gupta et al., U.S. Patent No. 5,845,100, has taught a method of aligning instructions using dual buffers and a rotator, transferring the instructions between various stages of buffers.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO

12/3/2003

EDDIE CHAN
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